

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE  
(MBHB Case No. 02-957)

In re Application of: )  
Rajmohana Hegde et al. )  
Serial No. 10/603,388 ) Examiner: TBD  
Filed: June 24, 2003 ) Art Unit: 2631  
For: Method and Apparatus for )  
Delayed Recursion Decoder )

INFORMATION DISCLOSURE STATEMENT

Commissioner for Patents  
P.O. Box 1450  
Alexandria, VA 22313-1450

Dear Sir:

Pursuant to 37 C.F.R. Section 1.97 - 1.99, the Applicant wishes to make the following references of record in the above-identified application. This Information Disclosure Statement is in compliance with the continuing duty of candor as set forth in 37 C.F.R. Section 1.56. Copies of the references cited below are enclosed. These references are also listed on the enclosed PTO Form 1449.

In the judgment of the undersigned, portions of the listed references may be material to the Examiner's consideration of the presently pending claims. However, the references have not been reviewed in sufficient detail to make any other representation and, in particular, no representation is intended as to the relative relevance between references, whether cited in this or prior statements. This statement is not a representation that the listed references have effective dates early enough to be "prior art" within the meaning of 35 U.S.C. Section 102 or Section 103.

## CITED REFERENCES

### **U.S. PATENT APPLICATION DOCUMENTS**

Document Number	Date	Name	Class	Filing Date If Appropriate
2001/0035994	02/28/2001	Agazzi et al.		11/01/2001
2001/0035997	01/17/2001	Agazzi		11/01/2001
2002/0012152	07/23/2001	Agazzi et al.		01/31/2002
2002/0080898	03/01/2002	Agazzi et al.		06/27/2002
2002/0060827	11/20/2001	Agazzi		05/23/2002

### **OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc).**

Lee, Edward A., Messerschmitt, David G., *Digital Communication-Second Edition*, pp. 406-409.

Sieben, Mike, Conradi, Jan, Dodds, David E., *Optical Single Sideband Transmission at 10 Gb/s Using Only Electrical Dispersion Compensation*, Journal of Lightwave Technology, Vol. 17 No. 10, pp. 1742-1749, October 1999.

Haykin, Simon S., *Adaptive Filter Theory*, pp. 8-10, 1986.

Kim, Kyoung, Powers, Edward J., *A Digital Method of Modeling Quadratically Nonlinear Systems with a General Random Input*, IEEE Transactions on Acoustics, Speech, and Signal Processing, vol. 36, no. 11, pp 1758-1769, November 1988.

Shanbhag, Naresh R., *Algorithms Transformation Techniques for Low-Power Wireless VLSI Systems Design*, pp. 1-36.

Fettweis, Gerhard, Meyr Heinrich, *High-Speed Parallel Viterbi Decoding: Algorithm and VLSI-Architecture*, IEEE Communications Magazine, pp. 46-55, May 1991.

Parhi K. Keshab, *Pipelining and Parallel Processing*, pp. 63-73, 1999.

Haunstein, Sticht K., *Design of Near Optimum Electrical Equalizers for Optical Transmissions In the Presence of PMD*.

Bulow, Henning, Thielecke, Tunther, *Electronic PMD Mitigation-From Linear Equalization to Maximum-Likelihood Detection*.

Boo, Montse, Arguello, Francisco, Bruguera, Javier D., Doallo Ramon, *High-Performance VLSI Architecture for the Viterbi Algorithm*, IEEE Transactions on Communications, Vol. 45, No. 2, pp. 168-176, February 1997.

Fettweis, Gerhard, Meyer, Heinrich, *Parallel Viterbi Algorithm Implementation: Breaking the ACS-Bottleneck*, IEEE Transactions on Communications, Vol. 37, No. 8, pp. 785-790, August 1989.

Tzou, Kou-Hu, Dunham, James G., *Sliding Block Decoding of Convolutional Codes*, IEEE Transactions on Communications, Vol. Com-29, No. 9, pp. 1401-1403, September 1981.

Robertson, Patrick, Hoeher, Peter, *Optimal and Sub-Optimal Maximum a Posteriori Algorithms Suitable for Turbo Decoding*, ETT Vol. 8, pp. 119-125, March-April 1997.

Black, Peter J., Meng, Teresa H., *A 140-Mb/s, 32-State, Radix-4 Viterbi Decoder*, IEEE Journal of Solid-State Circuits, Vol. 27, No. 12, pp. 1877-1885, December 1992.

Black, Peter J., Meng, Teresa H., *A 1-Gb/s, Four-State, Sliding Block Viterbi Decoder*, IEEE Journal of Solid-State Circuits, Vol. 32, No. 6, pp. 797-805, June 1997.

Fettweis, Gerhard, Meyr, Heinrich, *High-Rate Viterbi Processor: A Systolic Array Solution*, IEEE Journal on Selected Areas in Communications, Vol. 8, No. 8, pp. 1520-1534, October 1990.

A. K. Yeung and J. M. Rabaey, *A 210Mb/s Radix-4 Bit-level Pipelined Viterbi Decoder*, ISSCC, 1995.

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T.Conway, *Implementation of High Speed Viterbi Detectors*, Electronics Letters, 35(24):2089-2090, November 25 1999.

C. B. Shung, P. H. Siegel, G. Ungerboeck and H. K. Thapar, *VLSI architectures for metric normalization in the Viterbi algorithm*, in Proc. Int. Conf. Communications, vol. 4, Apr. 1990, pp. 1723-1728.

Hekstra, Andries P., *An Alternative to Metric Rescaling in Viterbi Decoders*, IEEE Transactions On Communications, Vol. 37, No. 11, pp. 1220-1222, November 1989.

In accordance with MPEP Sections 609 and 707.05(b), it is requested the documents cited (including any cited in applicant's specification which is not repeated on the attached Form PTO-1449) be given thorough consideration and that it be cited of record in the prosecution history of the present application by initialing on Form PTO-1449. Such initialing is requested even if the Examiner does not consider a cited document to be sufficiently pertinent to use in a rejection, or otherwise does not consider it to be prior art for any reason, or even if the Examiner does not believe that the guidelines for citation have been fully complied with. This is requested so that each document becomes listed on the face of the patent issuing on the present application.

Respectfully submitted,



Dated: October 21, 2003

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FORM PTO-1449  
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U.S. Department of Commerce  
Patent and Trademark Office

Atty. Docket No.

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02-957

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STATEMENT BY APPLICANT  
(Use several sheets if necessary)



Applicant:

Rajamohana Hegde et al.

Filing Date:

June 24, 2003

Group:

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	1.	2001/0035994	02/28/2001	Agazzi et al.			11/01/2001
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	5.	2002/0060827	11/20/2001	Agazzi			05/23/2002

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**FOREIGN PATENT DOCUMENTS**

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**OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc).**

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FORM PTO-1449 (Rev. 2-32)	U.S. Department of Commerce Patent and Trademark Office	Atty. Docket No. 02-957	Serial No. 10/603,388
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	8.	Haykin, Simon S., <i>Adaptive Filter Theory</i> , pp. 8-10, 1986.
	9.	Kim, Kyoung, Powers, Edward J., <i>A Digital Method of Modeling Quadratically Nonlinear Systems with a General Random Input</i> , IEEE Transactions on Acoustics, Speech, and Signal Processing, vol. 36, no. 11, pp 1758-1769, November 1988.
	10.	Shanbhag, Naresh R., <i>Algorithms Transformation Techniques for Low-Power Wireless VLSI Systems Design</i> , pp. 1-36.
	11.	Fettweis, Gerhard, Meyr Heinrich, <i>High-Speed Parallel Viterbi Decoding: Algorithm and VLSI-Architecture</i> , IEEE Communications Magazine, pp. 46-55, May 1991.
	12.	Parhi K. Keshab, <i>Pipelining and Parallel Processing</i> , pp. 63-73, 1999.
	13.	Haunstein, Sticht K., <i>Design of Near Optimum Electrical Equalizers for Optical Transmissions In the Presence of PMD</i> .
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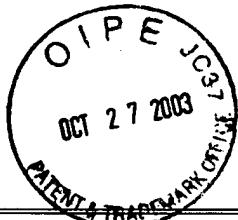
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	15.	Boo, Montse, Arguello, Francisco, Bruguera, Javier D., Doallo Ramon, <i>High-Performance VLSI Architecture for the Viterbi Algorithm</i> , IEEE Transactions on Communications, Vol. 45, No. 2, pp. 168-176, February 1997.
	16.	Fettweis, Gerhard, Meyer, Heinrich, <i>Parallel Viterbi Algorithm Implementation: Breaking the ACS-Bottleneck</i> , IEEE Transactions on Communications, Vol. 37, No. 8, pp. 785-790, August 1989.
	17.	Tzou, Kou-Hu, Dunham, James G., <i>Sliding Block Decoding of Convolutional Codes</i> , IEEE Transactions on Communications, Vol. Com-29, No. 9, pp. 1401-1403, September 1981.
	18.	Robertson, Patrick, Hoeher, Peter, <i>Optimal and Sub-Optimal Maximum a Posteriori Algorithms Suitable for Turbo Decoding</i> , ETT Vol. 8, pp. 119-125, March-April 1997.
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	20.	Black, Peter J., Meng, Teresa H., A 1-Gb/s, Four-State, Sliding Block Viterbi Decoder, IEEE Journal of Solid-State Circuits, Vol. 32, No. 6, pp. 797-805, June 1997.
	21.	Fettweis, Gerhard, Meyer, Heinrich, <i>High-Rate Viterbi Processor: A Systolic Array Solution</i> , IEEE Journal on Selected Areas in Communications, Vol. 8, No. 8, pp. 1520-1534, October 1990.
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	23.	Fettweis, Gerhard, Karabed, Razmik, Siegel, Paul H., Thapar, Hemant K., <i>Reduced-complexity Viterbi detector architectures for partial response signaling</i> , IEEE Global Telecommunications Conference, Singapore, Technical Program Conference Record, vol. 1, pp. 559-563, November 1995.
	24.	T.Conway, <i>Implementation of High Speed Viterbi Detectors</i> , Electronics Letters, 35(24):2089-2090, November 25 1999.
	25.	C. B. Shung, P. H. Siegel, G. Ungerboeck and H. K. Thapar, <i>VLSI architectures for metric normalization in the Viterbi algorithm</i> , in Proc. Int. Conf. Communications, vol. 4, Apr. 1990, pp. 1723-1728.
	26.	Hekstra, Andries P., <i>An Alternative to Metric Rescaling in Viterbi Decoders</i> , IEEE Transactions On Communications, Vol. 37, No. 11, pp. 1220-1222, November 1989.

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